This is a totally closed-book exam: No notes, books or magic genie are allowed.
CE: Question 1

(a) \( Y = A \cdot \overline{B} + \overline{A} \cdot B = A \text{XOR} B \)

(b) Unit cost (cheapest first): cell-based / PLA / FPGA

   Flexibility (most flexible first): FPGA / PLA / cell-based or FPGA / cell-based / PLA

   Performance (highest first): cell-based / FPGA / PLA or cell-based / PLA / FPGA

(c) \( P = C \cdot V^2 \cdot f \)

CE: Question 2

(a) \( \tau = \sum_{j=1}^{N} C_j \cdot \sum_{j=1}^{i} R_j = (1 \, \text{pF} \cdot 1 \, \text{k}\Omega) \cdot \sum_{j=1}^{N} i = 15 \, \text{ns} \)

(b) \( R = R_{sh} \cdot \frac{x}{y} \Rightarrow R = 600 \, \Omega \) when \( x = 120 \, \mu\text{m}, y = 4 \, \mu\text{m}, z = 3 \, \mu\text{m} \)

   \( R_{sh} \) (sheet resistance) = \( 600 \, \Omega / 30 = 20 \, \Omega \)

CE: Question 3

(a) A latch is level sensitive (i.e. transparent when clock is either high or low), while a flip flop is edge triggered.

(b) The signal propagating through combinational block 1 starts when \( \phi_1 \) goes high and has to reach the second latch at least the setup time before \( \phi_2 \) goes low. As a result: \( t_{sl} \leq 10 \, \text{ns} + 5 \, \text{ns} + 10 \, \text{ns} - 1 \, \text{ns} = 24 \, \text{ns} \).